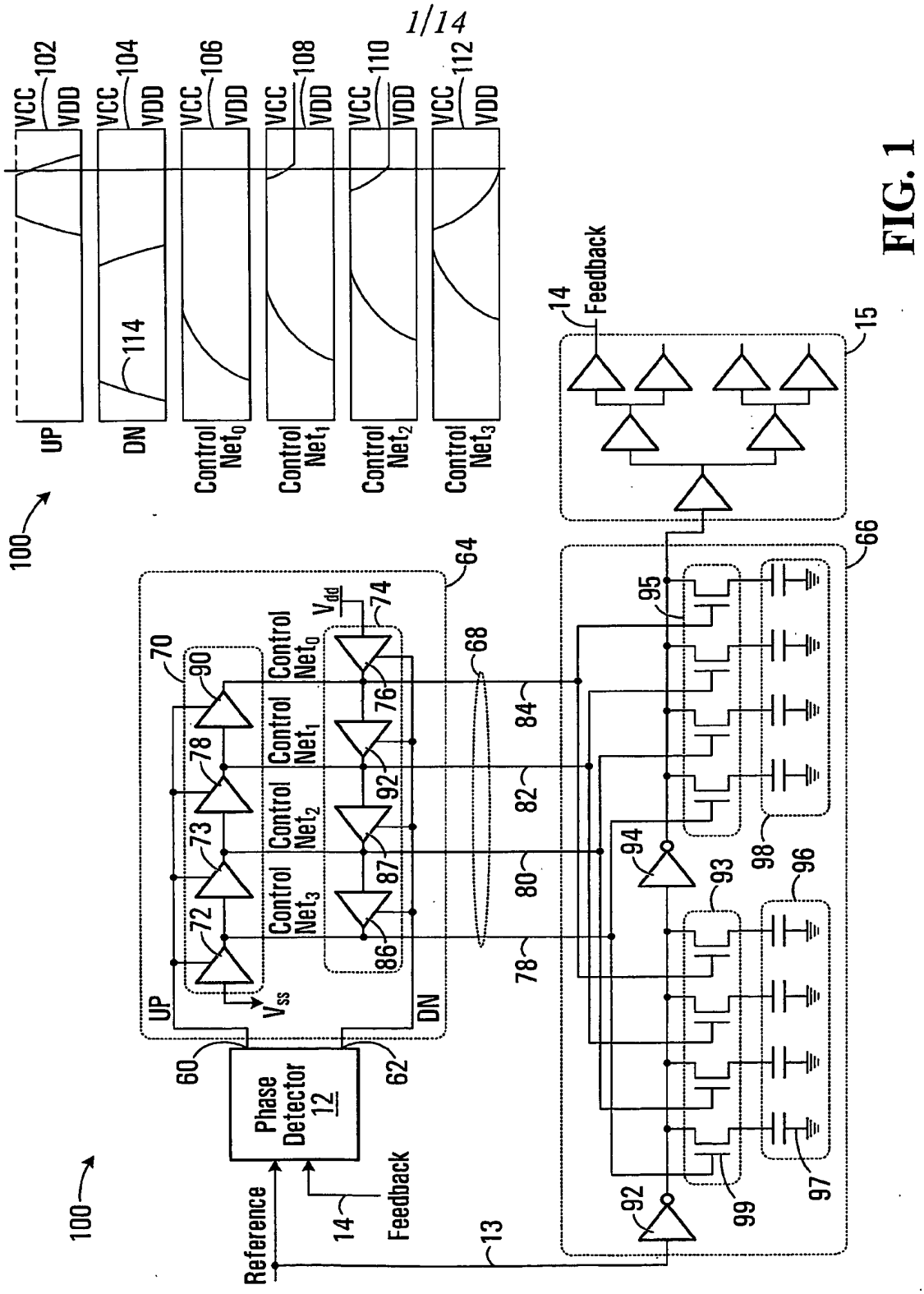
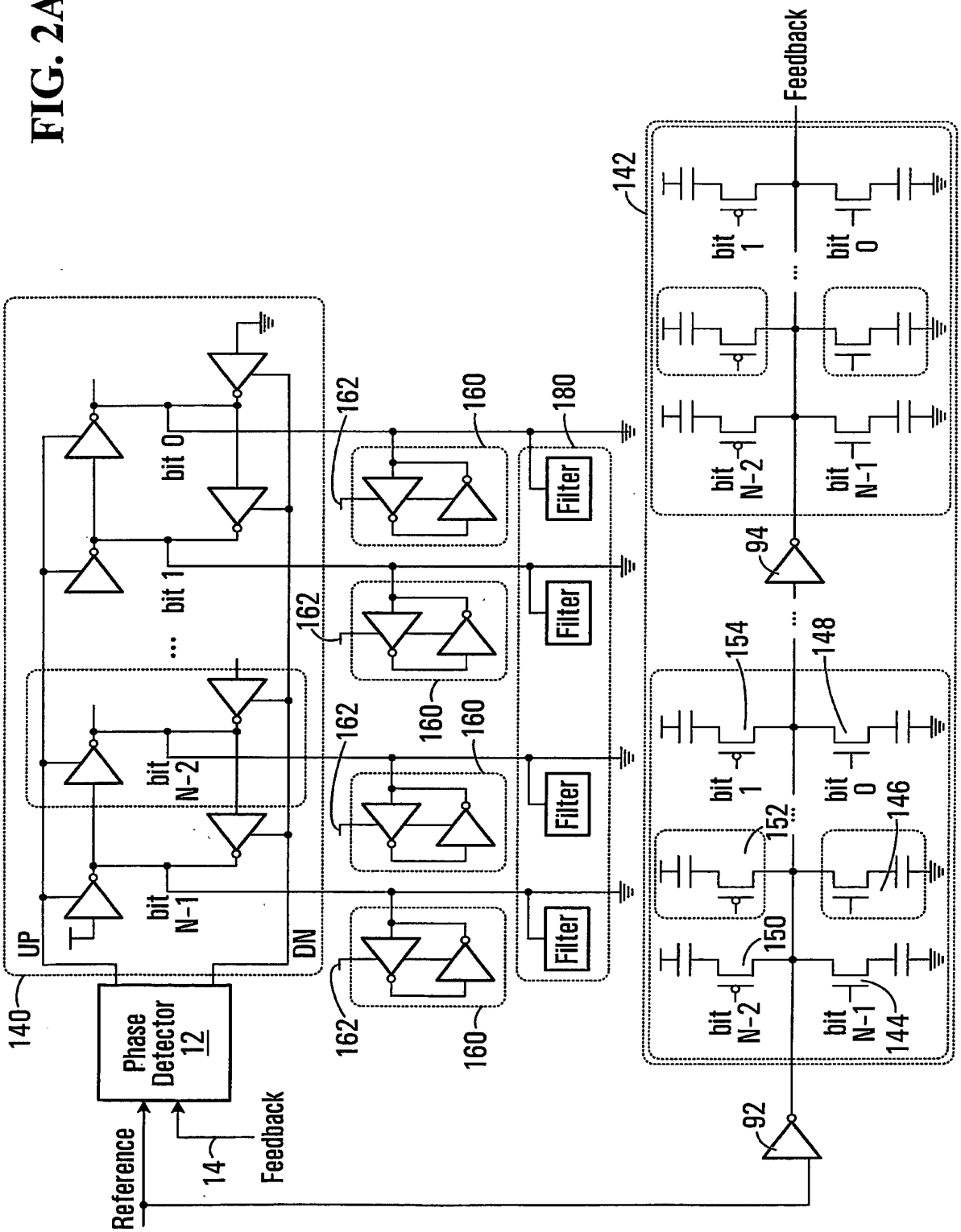

VCC
VDD
102
104
106
108
110
112
114
UP
DN
Control Net0
Control Net1
Control Net2
Control Net3
100
64
66
70
68
74
76
78
73
72
90
92
87
86
84
82
80
78
95
94
93
98
96
99
97
92
Vdd
Vss
Phase Detector 12
Reference
Feedback
14
15
13
60
62

FIG. 1

FIG. 2A


Feedback
142
bit 1
bit 0
bit N-2
bit N-1
94
154
148
152
146
150
144
92
162
160
180
Filter
140
UP
DN
Phase Detector 12
Reference
14
Feedback

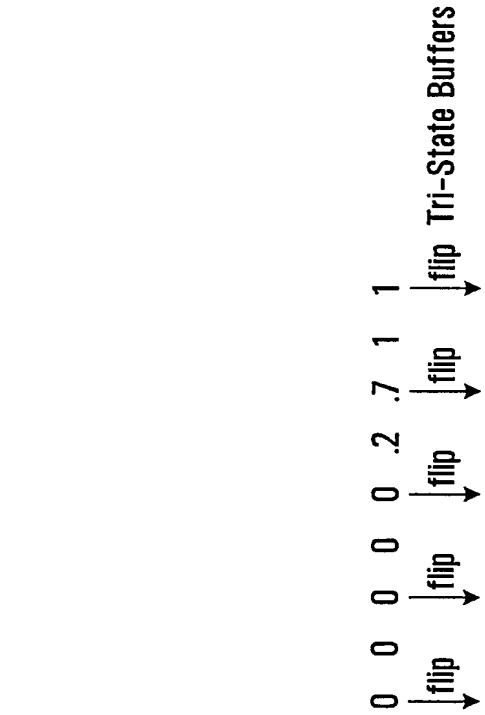

0 0 0 0 0 0 .2 .7 1 1
flip
flip
flip
flip
flip
flip
Tri-State Buffers

FIG. 2B

1 0 1 0 1 .2 .3 1 0
Inverters

FIG. 2C

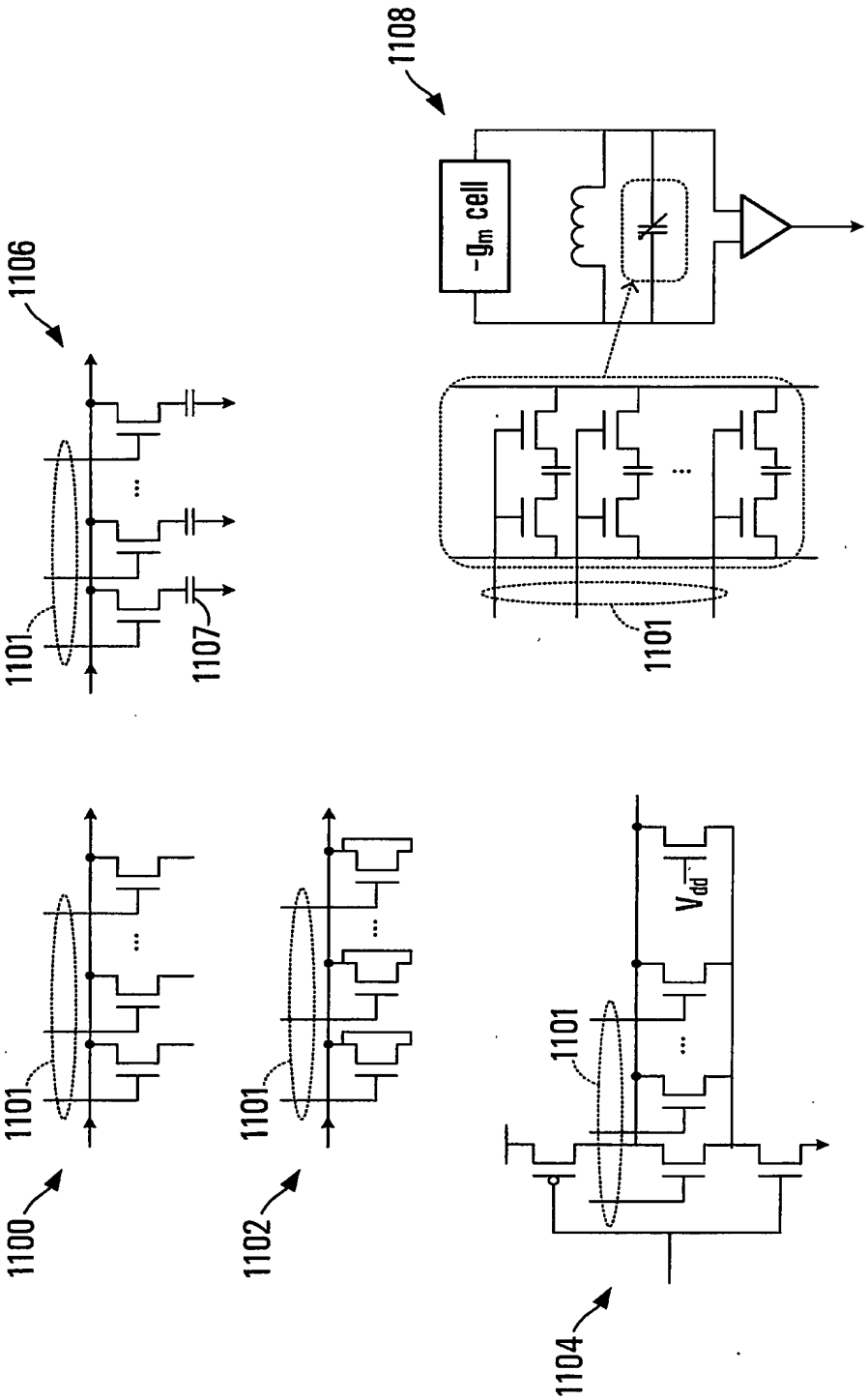


FIG. 2D

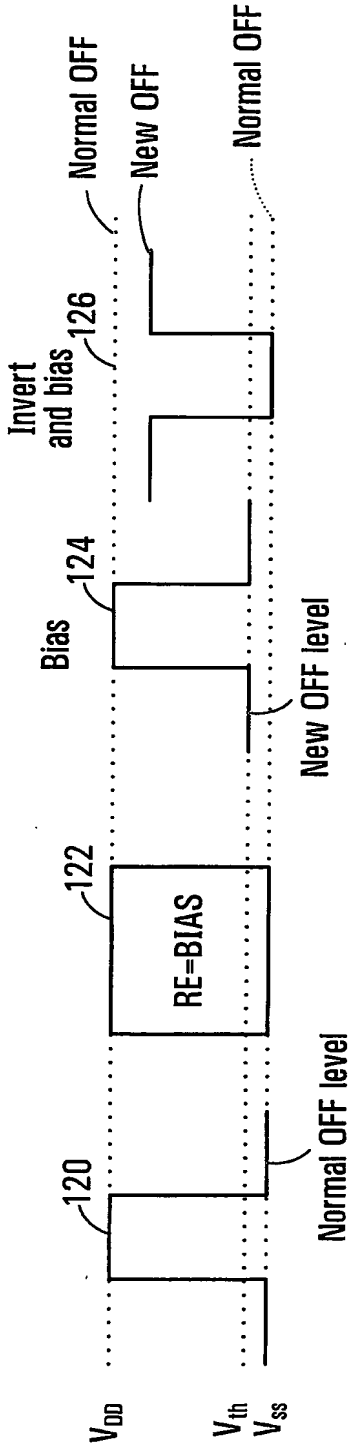
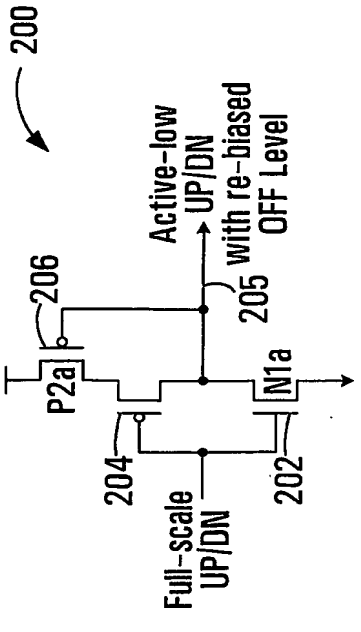

Normal OFF
New OFF
Normal OFF
Invert and bias
126
Bias
124
New OFF level
122
RE=BIAS
120
Normal OFF level
V_{DD}
V_{th}
V_{ss}

FIG. 3



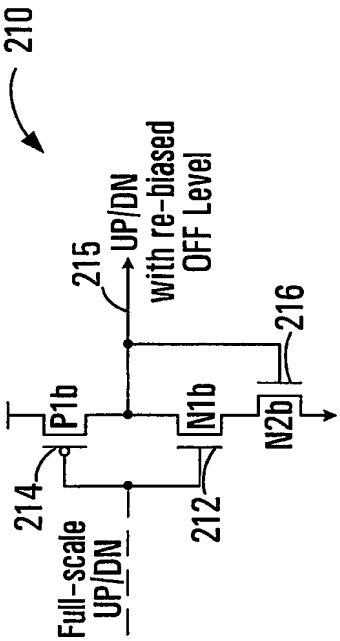


FIG. 4

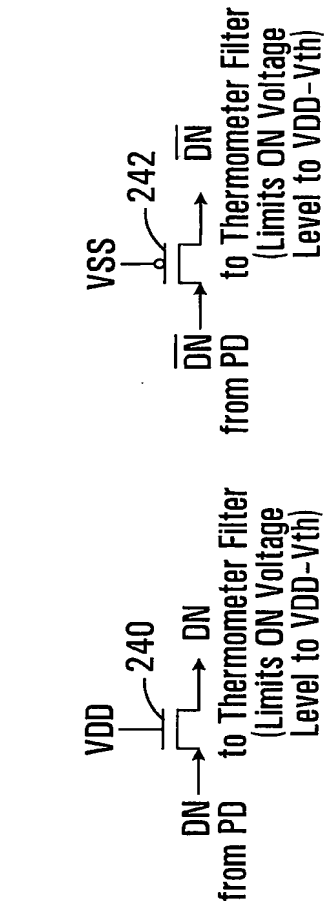


FIG. 6

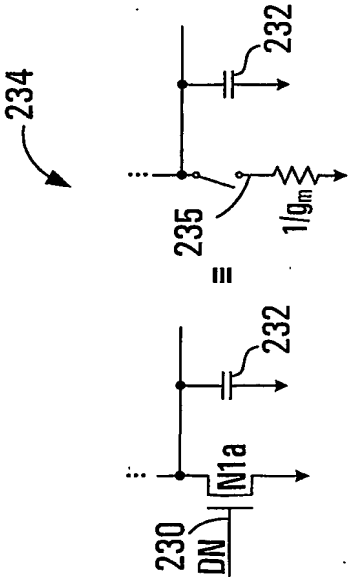


FIG. 5

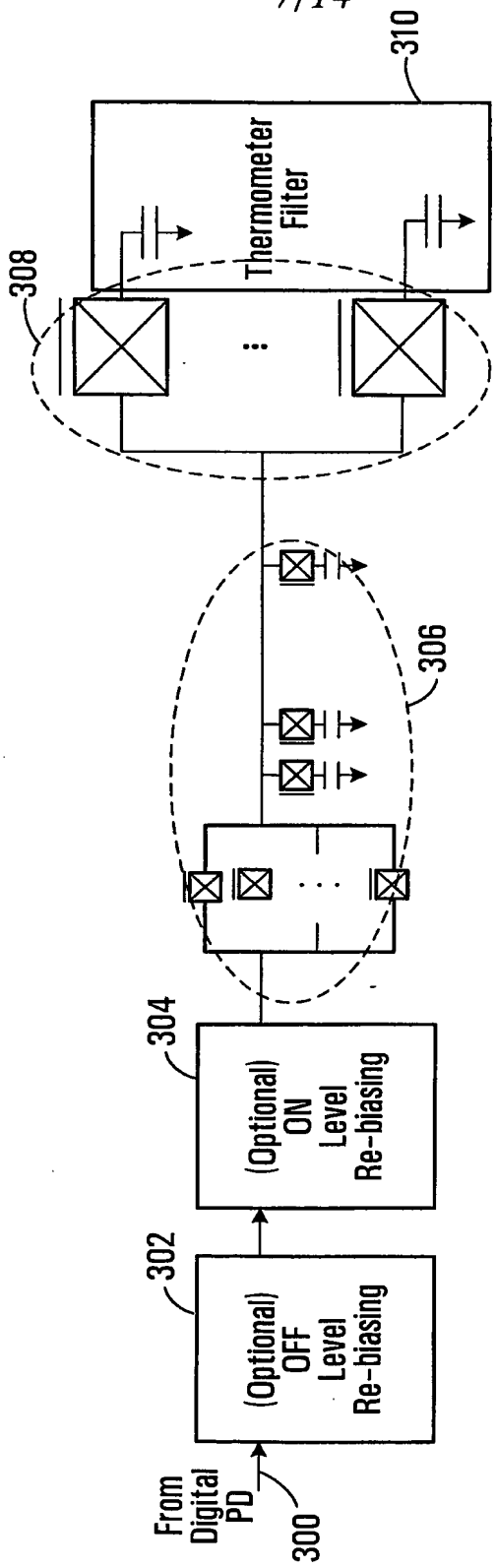

310
Thermometer Filter
308
306
304
(Optional) ON Level Re-biasing
302
(Optional) OFF Level Re-biasing
From Digital PD
300

FIG. 7

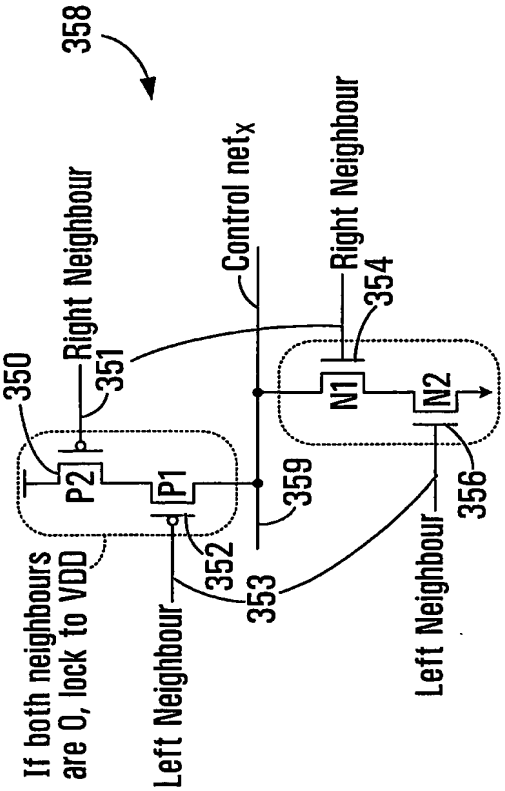

358
Right Neighbour
Control net$_X$
Right Neighbour
350
351
354
N1
N2
P2
P1
359
356
352
353
If both neighbours are 0, lock to VDD
Left Neighbour
Left Neighbour

FIG. 8A

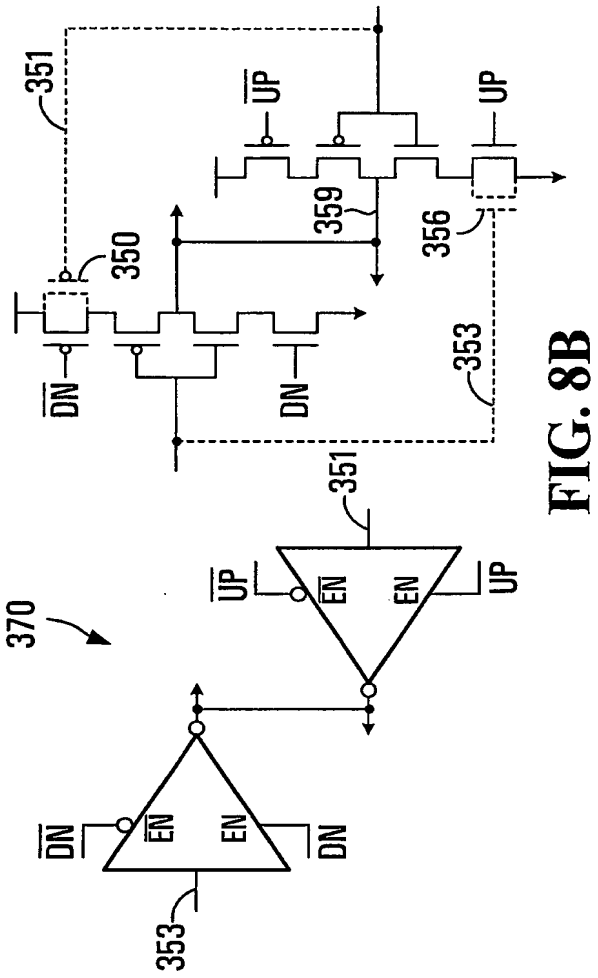

372
351
UP
UP
359
356
350
DN
DN
353
370
351
UP
EN
EN
UP
DN
EN
EN
DN
353

FIG. 8B

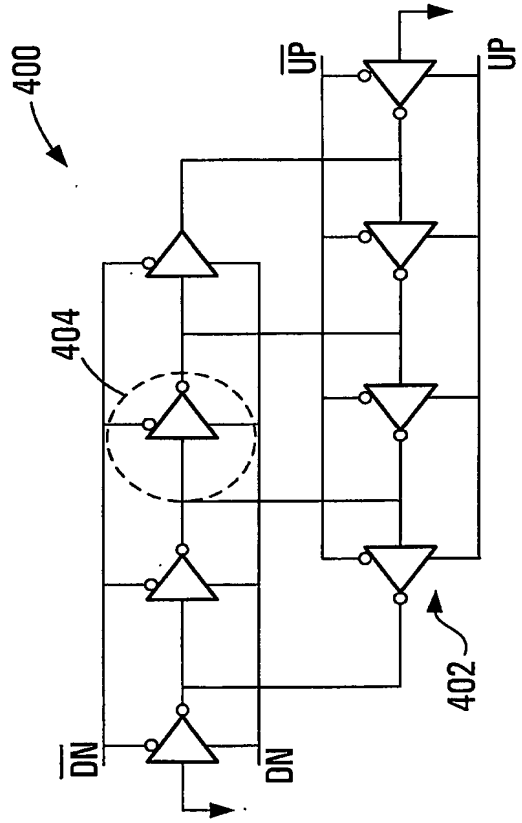
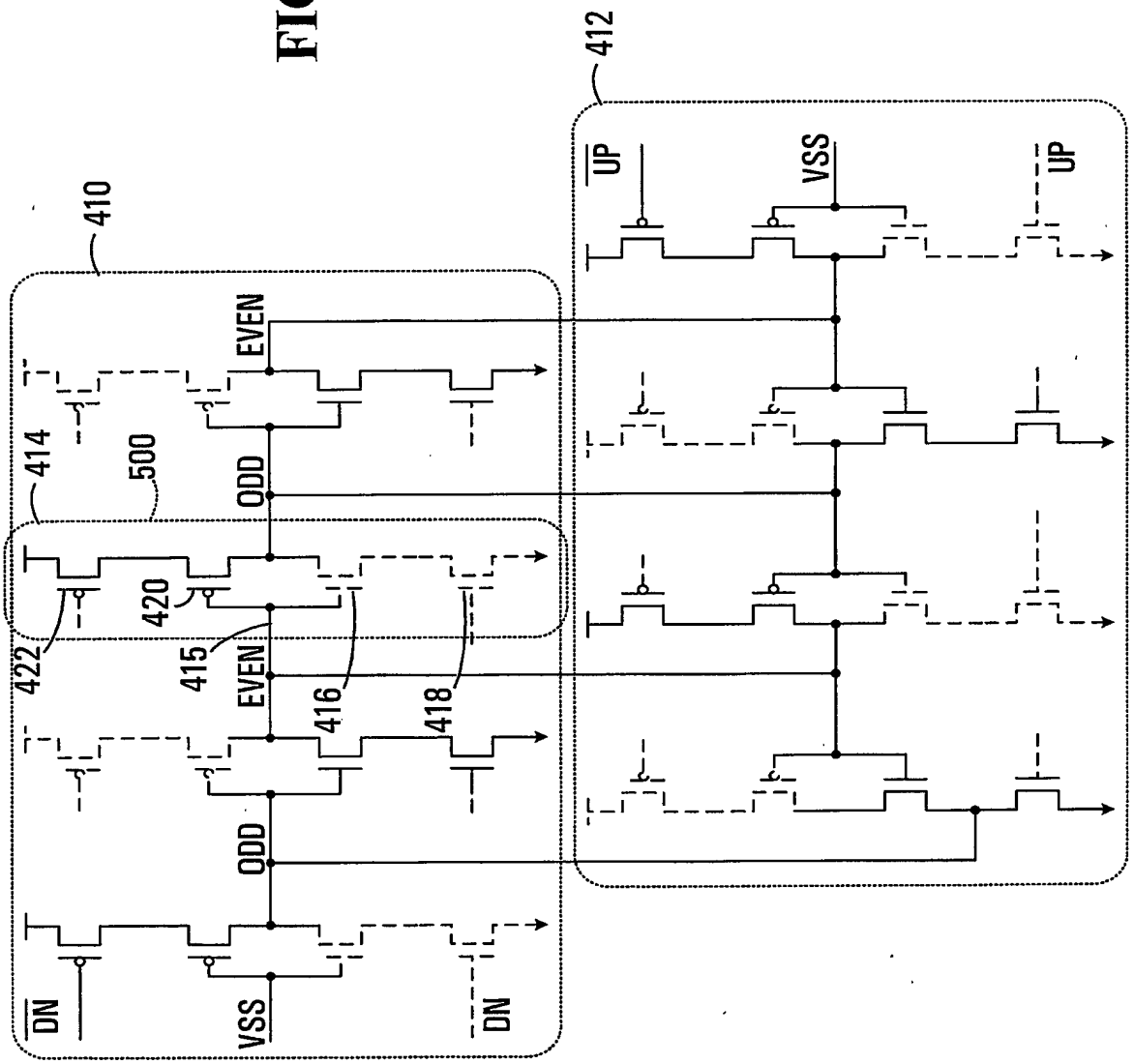


FIG. 9A

FIG. 9B


410
412
414
500
420
422
415
416
418
EVEN
ODD
EVEN
ODD
UP
VSS
UP
DN
VSS
DN

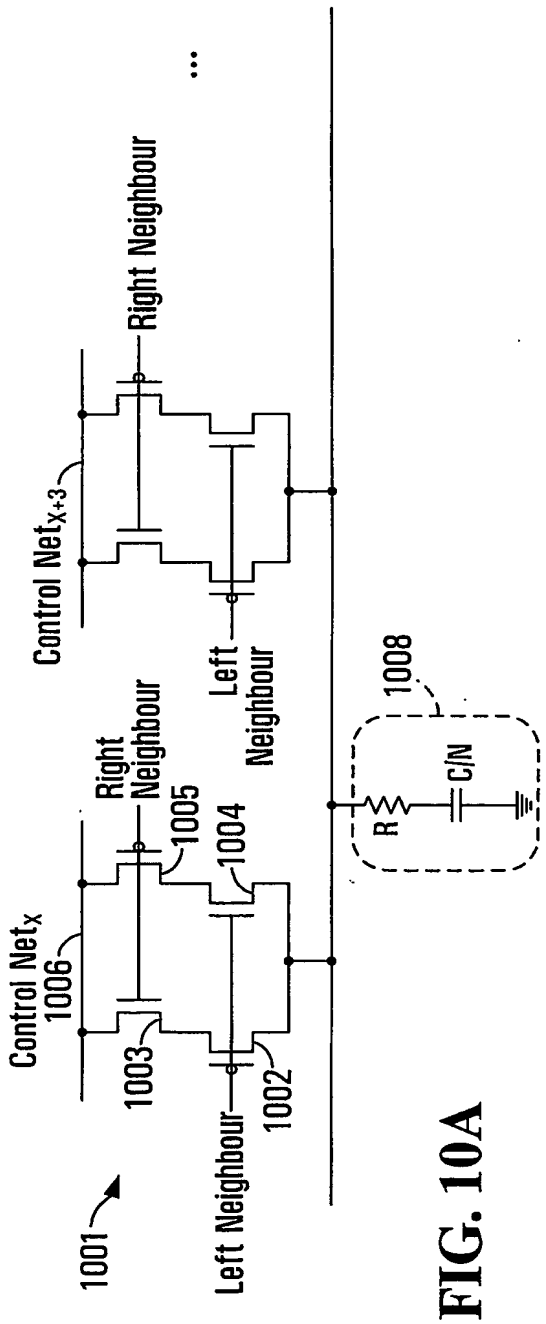


FIG. 10A

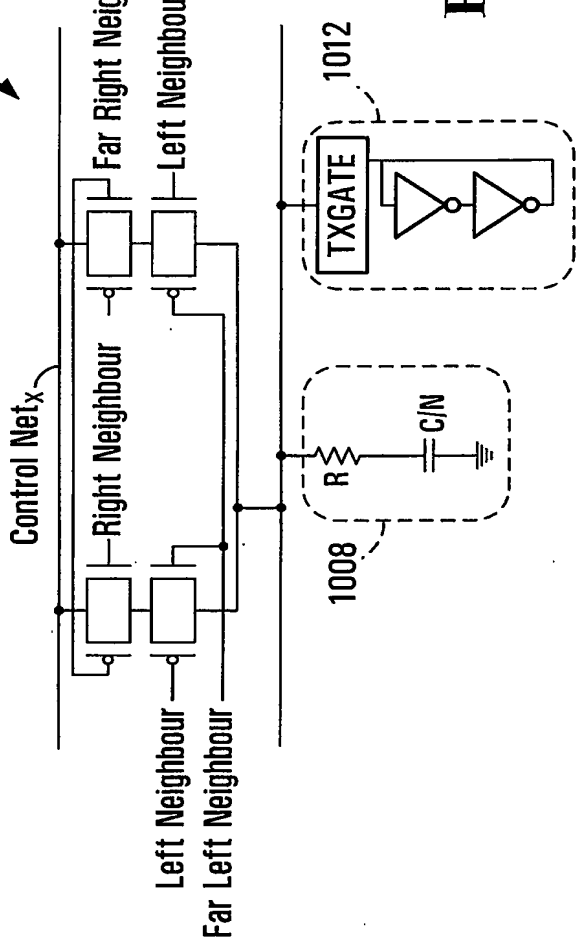


FIG. 10B

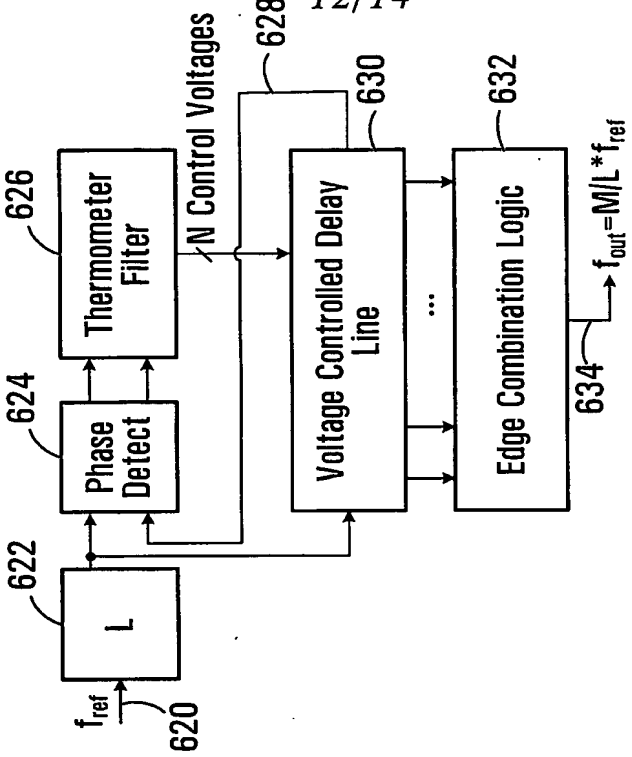

626
Thermometer Filter
N Control Voltages
628
630
632
624
Phase Detect
Voltage Controlled Delay Line
...
Edge Combination Logic
$f_{out}=M/L*f_{ref}$
634
622
L
620
f_{ref}

FIG. 12

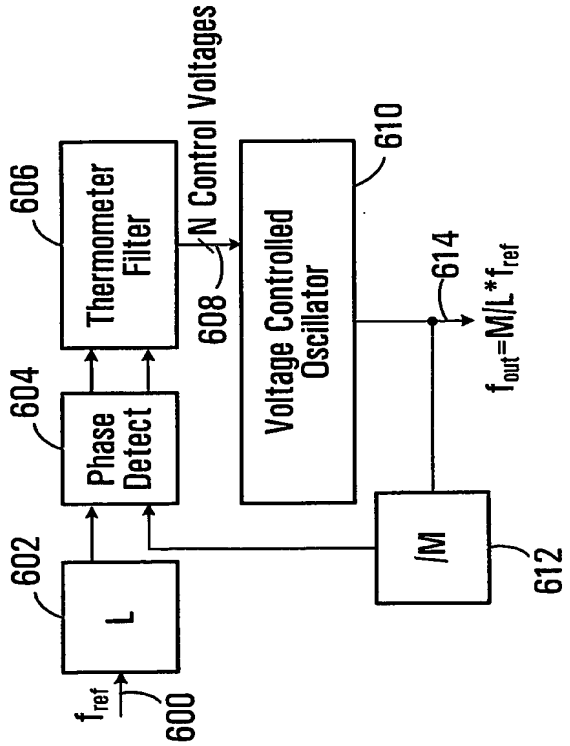

606
Thermometer Filter
N Control Voltages
608
610
604
Phase Detect
Voltage Controlled Oscillator
614
$f_{out}=M/L*f_{ref}$
602
L
/M
612
600
f_{ref}

FIG. 11

FIG. 13

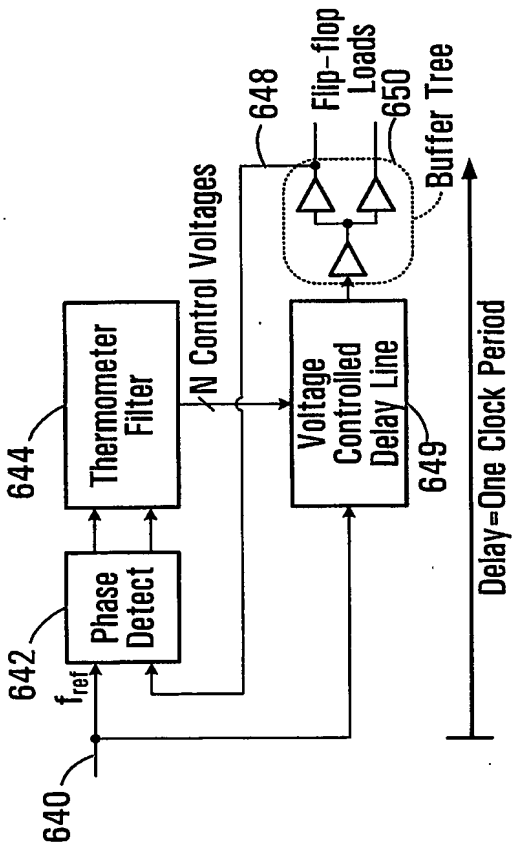
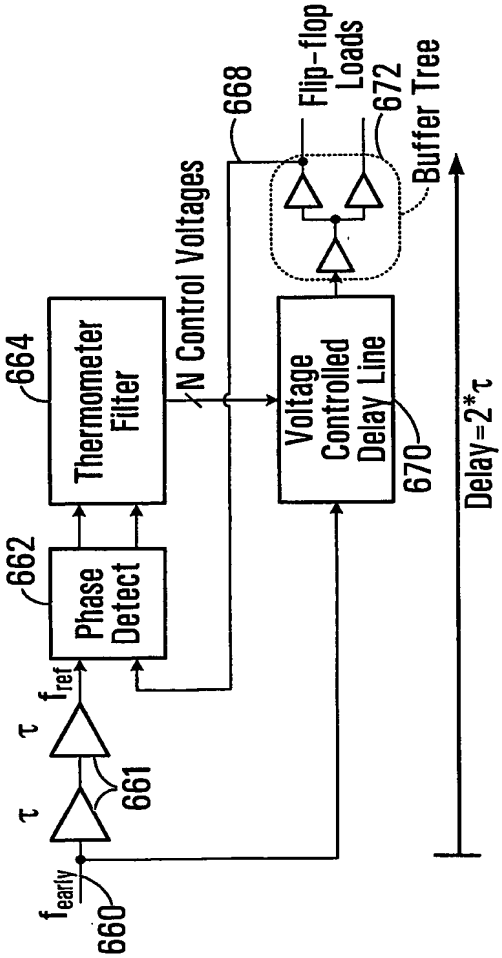

640
642
f_{ref}
Phase Detect
644
Thermometer Filter
N Control Voltages
648
Flip-flop Loads
650
Buffer Tree
Voltage Controlled Delay Line
649
Delay=One Clock Period

FIG. 14


660
f_{early}
τ
τ
661
f_{ref}
662
Phase Detect
664
Thermometer Filter
N Control Voltages
668
Flip-flop Loads
672
Buffer Tree
Voltage Controlled Delay Line
670
Delay=2*τ

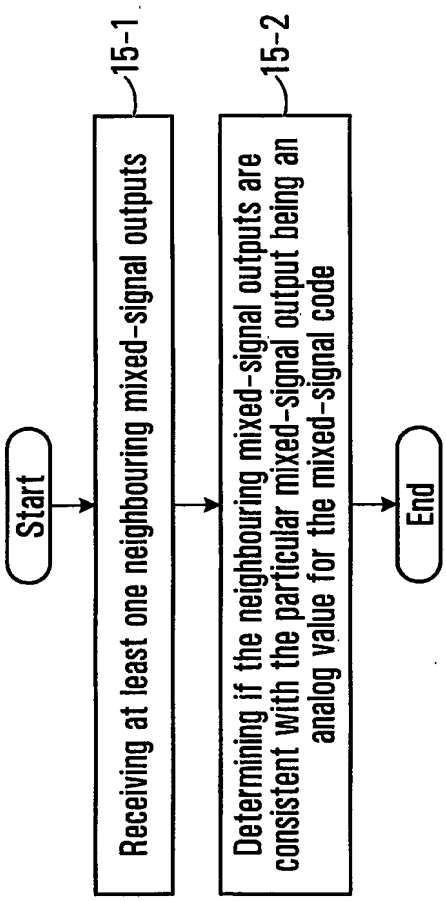

Start
15-1
Receiving at least one neighbouring mixed-signal outputs
15-2
Determining if the neighbouring mixed-signal outputs are consistent with the particular mixed-signal output being an analog value for the mixed-signal code
End

FIG. 15

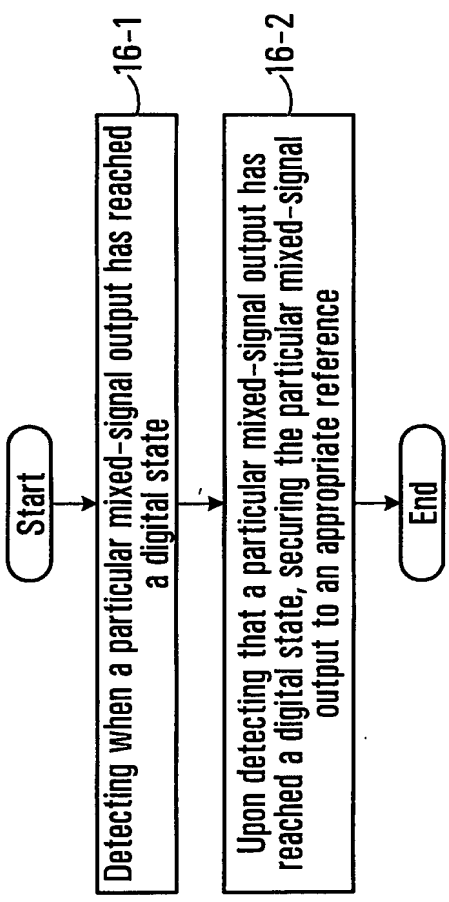

Start
16-1
Detecting when a particular mixed-signal output has reached a digital state
16-2
Upon detecting that a particular mixed-signal output has reached a digital state, securing the particular mixed-signal output to an appropriate reference
End

FIG. 16